PLATED SOURCE BRIDGE (PSB) GaAs POWER FET WITH IMPROVED RELIABILITY

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ABSTRACT

Flip chip type GaAs power FET having a plated source bridge (PSB) structure has been developed. Thermal resistance is improved by 2° C/W for a device with total gate width of 2400 μ. This improvement results in 2 times increase of the device MTTF. At the channel temperature of 150° C, MTTF more than 10^7 hours is estimated by accelerated operation life tests.

Introduction

In various microwave telecommunication systems or radar systems, replacement of TWT by GaAs power FET has been rapidly promoted aiming at improvement of reliability and reduction of equipment size.

Structure of existing GaAs power FETs is classified roughly into following four types.

1. cross over structure(1)
2. air bridged structure(2)
3. via hole structure(3)
4. flip chip structure(4)

In the cross over structure, high frequency operation above X band is difficult because of the parasitic capacitance of a dielectric material which is placed between electrodes for electric isolation. In the air bridged structure, high density integration of unit devices is difficult. In the via hole structure, difficulties to precisely adjust the positions of the source electrode and the corresponding via hole and to handle a thin GaAs wafer exist.

In the flip chip structure, performance at above X band frequencies is much improved by the minimized parasitics. However, in the conventional flip chip structure, as the source electrodes are separated each other, electrical probing is difficult. Overlooked defective FET chips often result in poor work efficiency and low production yield.

Considering the situation, a new technology to connect the source islands by a plated gold bridge has been developed. This new structure is called "Plated Source Bridge (PSB) structure", which has made possible to

1. probe electrically without difficulty
2. improve the work efficiency and the production yield
3. further improve the thermal resistance

Structure and Processing

Basing on our conventional flip chip structure shown in Fig. 1, PSB structure shown in Fig. 2 has been developed, where the source islands are connected by a thick gold bridge formed by electroplating.

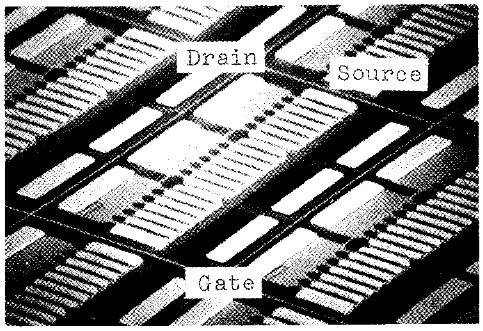

Fig. 1 Configuration of conventional flip chip device

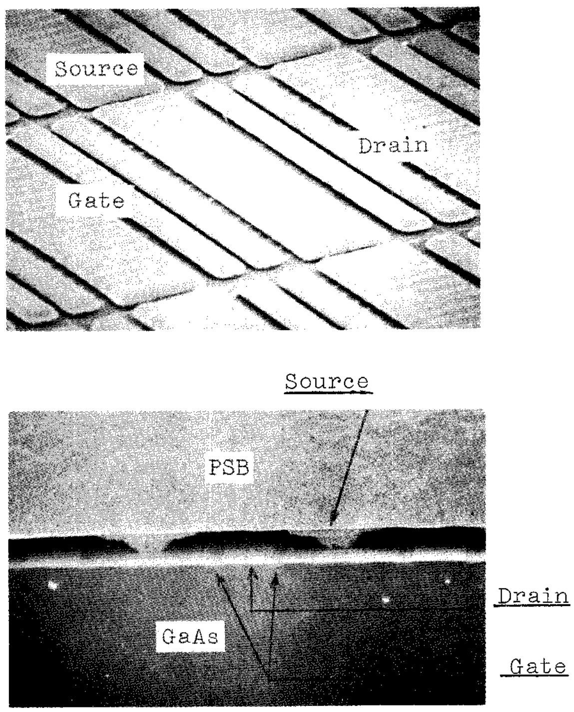

Fig. 2 Configuration (a) and cross section (b) of PSB device

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Technology to form the PSB structure is shown in Fig. 3. Only leaving the surface of the source islands, other area of the FET chip is completely covered with photoresist (Fig. 3-a). A thin metal layer for electroplating is placed all over the chip surface by evaporation, which is then covered with photoresist. Using a conventional photo-etching technique, windows to form the PSB at the desired portions are opend (Fig. 3-b). Gold bridge of 40 to 50 µ thick are formed on the exposed metal portions (Fig. 3-c). Finally, the photoresist is removed to obtain the structure shown in Fig. 3-d (Fig. 2).

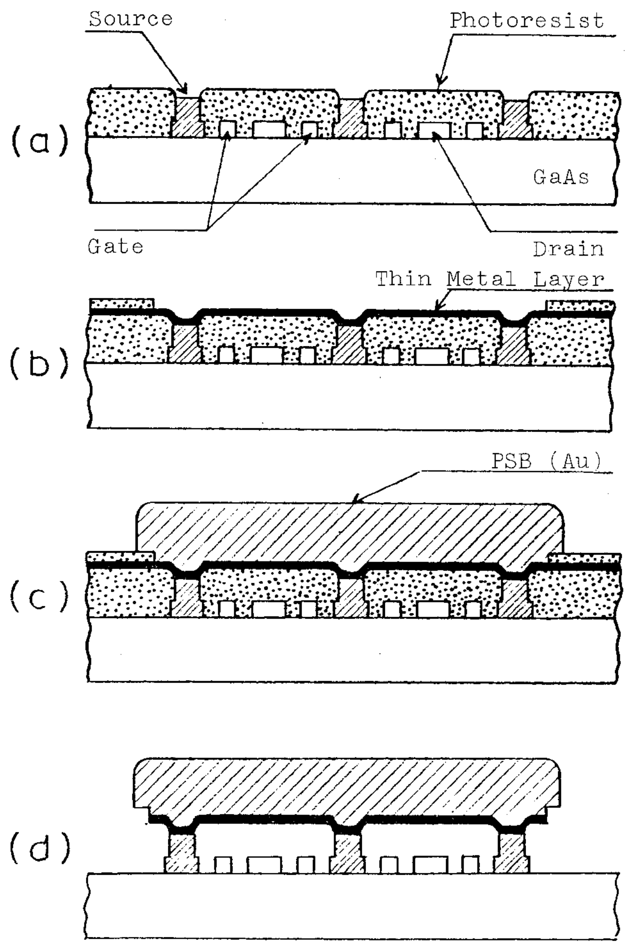

Fig. 3 Process to form PSB structure

Applying this technology to one of Mitsubishi commercially available devices, MGF-2124, PSB GaAs power FETs were fabricated. The doping level of the active layer was typically $1.8 \times 10^{17}/cm^3$. Source and drain were metallized with Au-Ge/Ni, which had a specific sheet resistivity less than $3 \times 10^{-7}\ \Omega\text{-cm}^2$. The spacing between the source and the drain electrodes was 4 µ. Aluminum gate was formed in a recess locating in the center between the source and the drain electrodes. The gate length, the unit gate width and the total gate width were 1 µ, 200 µ and 2400 µ, respectively.

The FET chip was mounted up side down in a package. The PSB was soldered to a package pedestal using Au-Ge alloy and the gate and the drain electrodes were connected to corresponding lead terminals with gold ribbons.
In the process, as only good FET chips selected by electrical probing were assembled, production yield and work efficiency were sharply improved.

Electrical Characteristics and Reliability

The PSB GaAs power FET modified from MGF-2124 typically showed following performance at 14 GHz under the bias conditions of V_{DS} = 8 V and I_D = 300 mA.

P_{1dB} = 0.75 W

G_P = 5.5 dB

η_{add} = 23 %

Regarding the performance, no conclusive improvement was obtained by the PSB structure compared with the conventional flip chip structure having equivalent device design parameters.

However, notable improvement was observed in thermal resistance of the device. In Fig. 4, typical thermal resistance is compared for the PSB devices and the conventional flip chip devices. In the PSB devices, improvement of the thermal resistance was typically 2 °C/W and thermal resistance less than 12 °C/W was reproducively obtained. This improvement was understood to have been brought on by the better contact and the strong adhesion between the source electrode and the package pedestal. Moreover, it should be noted in Fig. 4 that the distribution of the thermal resistance is so small for the PSB devices compared with the conventional flip chip devices.

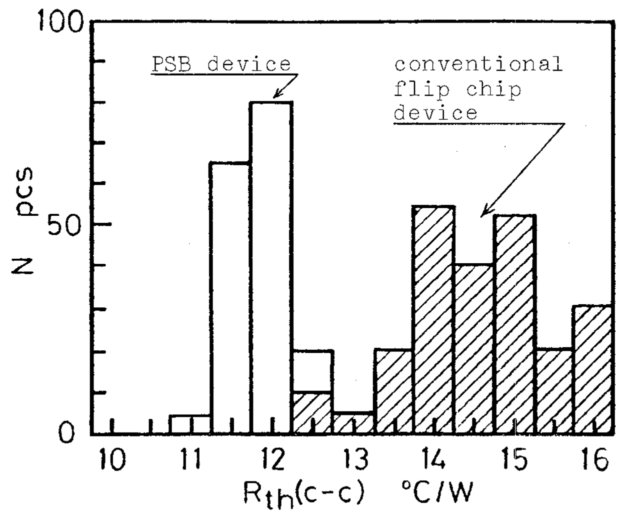

Fig. 4 Distribution of thermal resistance

In Fig. 5, MTTF of the device is shown as a function of the reciprocal value of the operation channel temperature both for the PSB device and the conventional flip chip device. The improvement of the thermal resistance of 2 °C/W resulted in 2 times increase of MTTF for the PSB device. At the channel temperature of 150 °C, MTTF of the PSB device has been estimated being more than 10^7 hours.

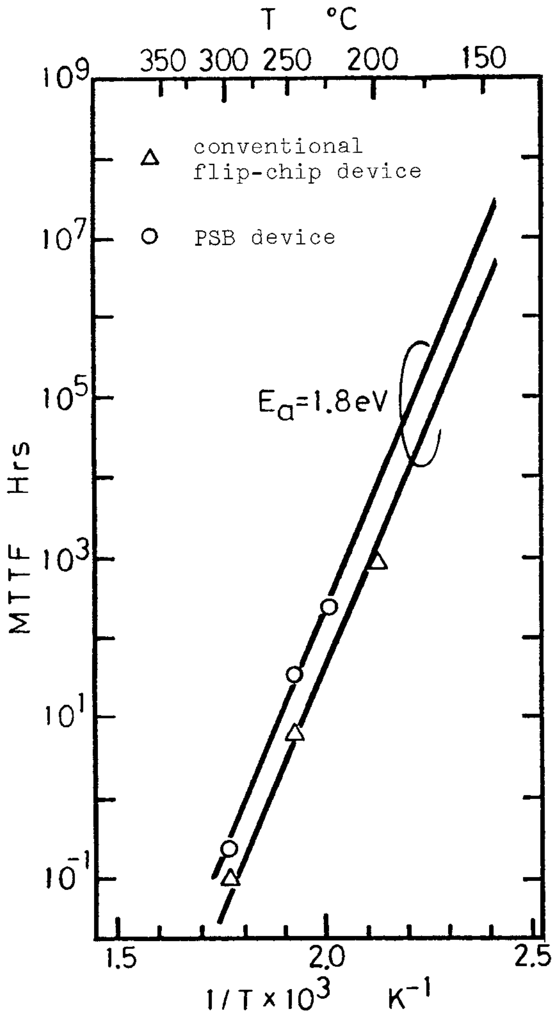

Fig. 5 MTTF vs 1/T obtained in operation life tests

Conclusion

On the basis of our conventional flip chip structure, a PSB GaAs power FET has been developed. In the PSB structure, so far isolated source electrodes are connected by a thick gold bridge formed by electroplating.

By the PSB structure,

1. electrical probing has become easy
2. only good FET chips are assembled and as the results, production yield and work efficiency has been sharply increased.

Modifying MGF-2124, PSB GaAs power FETs having total gate width of 2400 μ were fabricated. Typical performance of the fabricated devices was P_{1dB} = 0.75 W and G_p = 5.5 dB at 14 GHz. Thermal resistance was improved by 2 °C/W and decreased to 12 °C/W.

By the accelerated operation life tests, it was confirmed that this improvement of 2 °C/W had resulted in 2 times increase of MTTF for the PSB device compared with the conventional flip chip device. At the channel temperature of 150 °C, MTTF more than 10^7 hours has been estimated for the PSB device, which is understood to be enough for high reliability applications.

Acknowledgement

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